I CLAIM:

1. A signal processing system comprising:

- a system input for receiving an analog input signal;

- a system output for providing a digital output signal;

- signal processing path between the system input and the system output and comprising:

- analog signal processing means coupled to the system input for processing the analog signal;

- an analog-to-digital converter (ADC) with an ADC input and an ADC output, wherein:

- the ADC input is connected to the analog signal processing means for receiving the processed analog signal; and

- the ADC output provides a digital output signal indicative of the processed analog signal and is coupled to the system output;

- compensation means for reducing an offset level induced in the processed analog signal by the analog signal processing means, and comprising:

- first means connected to the system input for temporarily fixing a level of the analog signal at the system input; and

- second means connected to the ADC output for storing the output signal associated with the fixed level; and

- third means connected to the second means and to the signal processing path for affecting the signal processing after releasing the level, under control of the stored output signal.

2. The system of claim 1, wherein:

- the second means comprises a register for storing the output signal associated with the fixed level;

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- the third means comprises:

- a digital-to-analog converter (DAC) having a DAC input connected to the register, and having a DAC output for providing an analog correction signal under control of the stored output signal; and

- a modifying circuit having a first input connected to the DAC output for receipt of the correction signal, a second input connected to the analog signal processing means for receipt of the processed analog signal, and a circuit output coupled to the ADC input for providing the processed analog signal modified under control of the correction signal.

3. The system of claim 2, wherein

- the third means comprises an amplifier in the signal processing path having an amplifier output connected to the second input of the modifying circuit;

- the amplifier has first and second gain settings selectable through the first means.

4. The system of claim 3, wherein the third means comprises a second amplifier between the DAC and the first input of the modifying circuit.

5 The system of claim 2, wherein:

- the ADC comprises a flash analog-to-digital converter (FADC) having a ladder of resistors;

- the DAC comprises:

- an array of multiple switches, each respective one thereof coupled between a respective node in a respective pair of interconnected ones of the resistors and the first input of the modifying circuit; and

- control logic connected between the register and the array for selectively controlling the switches depending on the output signal stored in the register.

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6. The system of claim 5, wherein:

- the modifying circuit has a further input for receiving a further correction signal;

- the second means comprises a further array of multiple further switches, each respective one thereof coupled between a respective node in a respective pair of interconnected ones of the resistors and the further input; and

- the control logic is connected between the register and the further array for selectively controlling the further switches under control of the output signal stored in the register.

7. The system of claim 1, wherein the third means is connected to the signal processing path between the system output and the ADC output.

8. An electronic circuit with analog-to-digital converter means with a cascaded configuration, wherein the configuration comprises:

- a configuration input for receiving an analog input signal

- a configuration output for providing a digital output signal;

- first stage connected to the configuration input and comprising:

- a first ADC converter, being of the flash-type and having a ladder of resistors, and having a digital output for providing a digital output signal and an analog output for providing an analog output signal;

- an array of multiple switches, each respective one thereof coupled between a respective node in a respective pair of interconnected ones of the resistors and the analog output;

- a register connected to the digital output; and

- control logic connected between the register and the array for selectively controlling the switches depending on the output signal stored in the register;

- a second stage having:

- storing the digital output signal associated with the fixed level;

- releasing the level; and

- affecting the signal processing under control of the stored output signal after releasing the level.

13. The method of claim 12, wherein the affecting comprises:

- creating an analog correction signal on the basis of the stored digital output signal; and

- modifying the processing of the analog input signal under control of the correction signal.

14. The method of claim 13, comprising:

- amplifying the processed analog input signal by a first factor when the level is fixed;

- amplifying the processed analog signal by a second factor different from the first upon release of the level.

15. The method of claim 13, wherein:

- the converting comprises using a flash-ADC, the flash-ADC comprising a resistor ladder;

- the creating comprises selectively tapping in the resistor ladder under control of the stored digital output signal.

- a first analog input connected to the configuration input;

- a second analog input connected to the analog output;

- a combining circuit connected to the first and second analog inputs for providing, at a circuit output, a combination of analog signals received at the first and second analog inputs;

- a second ADC having an ADC input connected to the circuit output.

9. An electronic circuit comprising:

- an ADC with a flash analog-to-digital converter (FADC) having a ladder of resistors;

- an array of multiple switches, each respective one thereof coupled between a respective node in a respective pair of interconnected ones of the resistors and an output node.

10. The circuit of claim 9, comprising,

- control logic connected to the array for selectively controlling the switches.

11. The circuit of claim 9, wherein:

- the circuit comprises a further array of multiple further switches, each respective one thereof coupled between the respective node in the respective pair of interconnected ones of the resistors and a further output node.

12. A method of signal processing, the method comprising:

- receiving an analog input signal at an input;

- processing the analog input signal;

- converting the processed analog input signal into a digital output signal, the method further comprising:

- temporarily fixing a level of the analog input signal at the input;